CLAIMS

1. A bias control circuit for a bias circuit, said bias circuit being coupled to an amplifier transistor, and further including a first bias transistor, a second bias transistor, and a third bias transistor, a base of said amplifier transistor being coupled to an emitter of said second bias transistor, a base of said second bias transistor being coupled to a base of said first bias transistor and to a collector of said third bias transistor, a base of said third bias transistor being coupled to an emitter of said first bias transistor and to said bias control circuit at a first node, said bias control circuit comprising:

means for receiving a control voltage; and

means for actively adjusting an equivalent resistance of said bias control circuit responsive to said control voltage, said equivalent resistance being established between said first node and a reference voltage.

2. The bias control circuit of claim 1, wherein said equivalent resistance is gradually decreased when said control voltage is increased.

3. The bias control circuit of claim 1, wherein a current drawn by said bias control circuit is gradually increased when said control voltage is increased.

4. The bias control circuit of claim 1, wherein a quiescent current of said amplifier transistor is gradually increased when said control voltage is increased.

5. The bias control circuit of claim 1, wherein said bias control circuit, said bias circuit and said amplifier transistor are integrated into a single die.

6. The bias control circuit of claim 1, wherein said amplifier transistor is a high-power CDMA transistor.

7. The bias control circuit of claim 1, wherein said reference voltage is ground.

8. A bias control circuit for a bias circuit, said bias circuit being coupled to an amplifier transistor, and further including a first bias transistor, a second bias transistor, and a third bias transistor, a base of said amplifier transistor being coupled to an emitter of said second bias transistor, a base of said second bias transistor being coupled to a base of said first bias transistor and to a collector of said third bias transistor, a base of said third bias transistor being coupled to an emitter of said first bias transistor and to said bias control circuit at a first node, said bias control circuit comprising:

a bias control transistor having a base, a collector, and an emitter;

a first resistor connected across said collector of said bias control transistor and said first node;

a second resistor connected across said collector of said bias control transistor and a first reference voltage;

a third resistor connected across said emitter of said bias control transistor and said first reference voltage; and

a fourth resistor connected across a control voltage and said base of said bias control transistor, wherein said bias control transistor actively adjusts an equivalent resistance of said bias control circuit responsive to said control voltage, said equivalent resistance being established between said first node and said first reference voltage.

9. The bias control circuit of claim 8, wherein each of said amplifier transistor, said first bias transistor, said second bias transistor, said third bias transistor and said bias control transistor comprises a bipolar transistor.

10. The bias control circuit of claim 9, wherein said amplifier transistor, said first bias transistor, said second bias transistor, said third bias transistor and said bias control transistor are integrated into a single die.

11. The bias control circuit of claim 8, further comprising a fifth resistor connected across said base of said first bias transistor and a second reference voltage, and a sixth resistor connected across said emitter of said second bias transistor and said first reference voltage.

12. The bias control circuit of claim 8, further comprising a temperature compensation

circuit comprising a fifth resistor and at least one diode, wherein a first end of said fifth resistor is connected to said base of said bias control transistor, a second end of said fifth resistor is connected to an anode of said at least one diode, a cathode of said at least one diode being connected to said first reference voltage.

13. The bias control circuit of claim 12, wherein said at least one diode comprises an HBT diode.

14. The bias control circuit of claim 8, further comprising a temperature compensation circuit comprising a fifth resistor and first and second Schottky diodes, wherein a first end of said fifth resistor is connected to said base of said bias control transistor, a second end of said fifth resistor is connected to an anode of said first Schottky diode, a cathode of said first Schottky diode being connected to an anode of said second Schottky diode, a cathode of said second Schottky diode being connected to said first reference voltage.

15. A bias control circuit for a bias circuit, said bias circuit being coupled to an amplifier transistor, and further including a first bias transistor, a second bias transistor, and a third bias transistor, a base of said amplifier transistor being coupled to an emitter of said second bias transistor, a base of said second bias transistor being coupled to a base of said first bias transistor and to a collector of said third bias transistor, a base of said third bias transistor being coupled to an emitter of said first bias transistor and to said bias

control circuit at a first node, said bias control circuit comprising:

a bias control transistor having a base, a collector, and an emitter;

a first resistor connected across said collector of said bias control transistor and said first node;

a second resistor connected across said collector of said bias control transistor and said emitter of said bias control transistor;

a third resistor connected across said emitter of said bias control transistor and said first reference voltage;

a fourth resistor connected across said emitter of said bias control transistor and an anode of a first diode, said first diode having a cathode connected to said first reference voltage;

a fifth resistor connected across a control voltage and said base of said bias control transistor, wherein said bias control transistor actively adjusts an equivalent resistance of said bias control circuit responsive to said control voltage, said equivalent resistance being established between said first node and said first reference voltage.

16. The bias control circuit of claim 15, wherein each of said amplifier transistor, said first bias transistor, said second bias transistor, said third bias transistor, and said bias control transistor comprises a bipolar transistor.

17. The bias control circuit of claim 16, wherein said amplifier transistor, said first

bias transistor, said second bias transistor, said third bias transistor, and said bias control transistor are integrated into a single die.

18. The bias control circuit of claim 15, further comprising a sixth resistor connected across said base of said first bias transistor and a second reference voltage, and a seventh resistor connected across said emitter of said second bias transistor and said first reference voltage.

19. The bias control circuit of claim 15, further comprising a temperature compensation circuit comprising a sixth resistor and at least one additional diode, wherein a first end of said sixth resistor is connected to said base of said bias control transistor, a second end of said sixth resistor is connected to an anode of said at least one additional diode, a cathode of said at least one additional diode being connected to said first reference voltage.

20. The bias control circuit of claim 15, wherein said first reference voltage is ground.